IN THE SPECIFICATION

Please replace paragraph [0002] with the following paragraph:

[0002] A content addressable memory CAM architecture is an array of individual CAM cells. Each CAM cell consists of a data storage unit and comparison circuitry. The storage unit is used for storing data and the comparison circuitry is used to compare the compare-data with the data stored in storage unit and providing a signal indicating a match or mismatch. This signal is fed to a priority encoder for selecting one of the match signals, in the event of multiple signals, as the final output.

Please replace paragraphs [0017] and [0018] with the following paragraphs:

[0017] For the combined compare and write operation, the address decoding and comparing are performed in the first half of the clock cycle. In the second half of the clock cycle the ~~world~~ word line corresponding to the decoded address is enabled and the Write driver then performs the write operation.

[0018] For the combined compare and read operation, the address decoding and comparing are performed in first half of the clock cycle. In the second half of the clock cycle the ~~world~~ word line corresponding to the decoded address is enabled, to provide the data contained in the memory at the bit lines. The data at the bit lines is then sensed by a sense amplifier. The output of sense amplifier is latched in the output latch.

Please replace paragraph [0021] with the following paragraph:

[0021] Figure 6 shows the timing diagram of a normal read operation. [[=]]As shown in the figure Comp_En is disabled on the positive edge of the clock cycle[[, ,]] and read enable line Read_En is enabled. The decoder provides the Address of the memory to be read, and when the complete address is available the Word Line corresponding to the decoded address is enabled thereby providing data content in the memory cell to the bit lines. The data is sensed by a sense amplifier and made available at the Data Out.

Please replace paragraphs [0023]-[0025] with the following paragraphs:

[0023] Figure 8 shows the timing diagram for a normal compare operation. As shown in the ~~figur~~ figure, Comp_En is enabled at the positive edge of the clock cycle, and, the compare data signal Comp_Data is enabled providing the data at the bit lines. Depending upon Match/mis-Match a hit/miss is generated.

[0024] Figure 9 shows the timing diagram for a combined compare and read operation[[.]]. In the positive phase of the clock cycle, the compare and decoding operation are performed generating a hit/miss signal. The hit/miss signal is latched for each row of the core at the falling edge of the clock. The address decoder is also activated at the positive edge of the clock for selecting a word line for the read operation from the memory. The Address is decoded for the output of the Predecoder stage or the input of the final decoder stage. The negative clock

cycle triggers the reading ~~action~~ action, enables the final ~~decoder~~ decoder, and selects the wordline corresponding to the address for the read operation.

[0025] Figure 10 shows the timing diagram for the combined compare and write operation. The compare and decoding operations are performed at the positive phase of clock generating a hit/miss signal. The hit/miss signal is latched for each row of the core at the falling edge of the clock. The positive phase of clock also activates the address decoder for selecting a word line for the write operation from the memory. The Address is decoded ~~upto~~ up to the output of the Predecoder stage or the input of the final decoder stage. The negative edge of the clock cycle triggers the writing ~~action~~ action, enables the final ~~decoder~~ decoder, and selects the wordline corresponding to the address input for the write operation.